L Number	Hits	Search Text	DB	Time stamp
1	20906	cache	USPAT	2002/03/09 17:20
2	0	cache. with eeprom	USPAT; DERWENT; IBM TDB	2002/03/09 17:21
3	116	cache with eeprom	USPAT; DERWENT; IBM TDB	2002/03/09 17:29
4	0	@pd<10890413 and (cache with eeprom)	USPAT; DERWENT; IBM TDB	2002/03/09 17:22
5	0	@pd<19890413 and (cache with eeprom)	USPAT; DERWENT; IBM TDB	2002/03/09 17:23
6	0	@pd<19900413 and (cache with eeprom)	USPAT; DERWENT; IBM TDB	2002/03/09 17:23
7	2	@pd<19910413 and (cache with eeprom)	USPAT; DERWENT; IBM TDB	2002/03/09 17:29
8	228	cache same eeprom	USPAT; DERWENT; IBM TDB	2002/03/09 17:29
9	9	@pd<19910413 and (cache same eeprom)	USPAT; DERWENT; IBM TDB	2002/03/09 17:52
10	1280	(cache near2 buffer) same (read$ or write$1 or writing or transfer or written$) same (memory or ram or eeprom or eprom or rom or prom)	USPAT; DERWENT; IBM TDB	2002/03/09 17:52
11	106	@pd<19890413 and ((cache near2 buffer) same (read$ or write$1 or writing or transfer or written$) same (memory or ram or eeprom or eprom or rom or prom))	USPAT; DERWENT; IBM TDB	2002/03/09 17:53
12	12244	711/$.ccls.	USPAT; DERWENT; IBM TDB	2002/03/09 18:00
14	23	eeprom same ((cache near2 buffer) same (read$ or write$1 or writing or transfer or written$) same (memory or ram or eeprom or eprom or rom or prom))	USPAT; DERWENT; IBM TDB	2002/03/09 17:59
15	0	((@pd<19890413 and ((cache near2 buffer) same (read$ or write$1 or writing or transfer or written$) same (memory or ram or eeprom or eprom or rom or prom))) and 711/$.ccls.) and (eeprom same ((cache near2 buffer) same (read$ or write$1 or writing or transfer or written$) same (memory or ram or eeprom or eprom or rom or prom)))	USPAT; DERWENT; IBM TDB	2002/03/09 17:59
16	7	(711/126.ccls. or 711/135.ccls. or 711/136.ccls. or 711/140.ccls. or 711/142.ccls.) and ((@pd<19890413 and ((cache near2 buffer) same (read$ or write$1 or writing or transfer or written$) same (memory or ram or eeprom or eprom or rom or prom))) and 711/$.ccls.)	USPAT; DERWENT; IBM TDB	2002/03/09 18:03
13	53	(@pd<19890413 and ((cache near2 buffer) same (read$ or write$1 or writing or transfer or written$) same (memory or ram or eeprom or eprom or rom or prom))) and 711/$.ccls.	USPAT; DERWENT; IBM TDB	2002/03/09 18:43
17	1611	((eeprom or eprom or prom or rom) with memory) same cache	USPAT; DERWENT; IBM TDB	2002/03/09 18:44
18	8	(((eeprom or eprom or prom or rom) with memory) same cache) and (@pd<19890413 and ((cache near2 buffer) same (read$ or write$1 or writing or transfer or written$) same (memory or ram or eeprom or eprom or rom or prom)))	USPAT; DERWENT; IBM TDB	2002/03/09 18:45

US-PAT-NO: 4466059
DOCUMENT-IDENTIFIER: US 4466059 A
TITLE: Method and apparatus for limiting data occupancy in a cache
DATE-ISSUED: August 14, 1984
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bastian; Arlon L.	Pima County	AZ	N/A	N/A
Goldfeder; Marc E.	Tucson	AZ	N/A	N/A
Hartung; Michael H.	Pima County	AZ	N/A	N/A

US-CL-CURRENT: 711/122
ABSTRACT:
A storage hierarchy has a backing store and a caching buffer store. During a series of accesses to the hierarchy by a user, writing data to the hierarchy results in data being selectively removed from the buffer store. Space in said buffer store not being allocated to data being written results in such data being written to the backing store to the exclusion of the buffer store. Removal of data increases the probability of writing data to the backing store. In a preferred implementation, the backing store is one or more disk type data storage apparatus and the buffer store is an electronic random access memory.
35 Claims, 3 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

ISD:
19840814

DEPR:
Referring now more particularly to the drawing, like numerals indicate like parts and structural features in the various diagrams. Using units 10, such as central processing units and the like, are coupled via input/output connections 11 to a storage hierarchy having a storage director 12, and preferably in the form of a peripheral data storage system. The storage hierarchy includes a backing store 14 and a **cache, or caching buffer** store, 15. Data is transferred between the backing store 14 and cache 15 via a set of device connections 13. Selectively, using units 10 can access cache 15 or backing store 14 in accordance with switch 17, 18 settings. For example, switch 17 set as shown couples output bus 20 of input/output connections 11 to device input connections 21 for transferring data from using units 10 directly to backing store 14. Backing store 14 supplies data directly to using units 10 via device output bus 22 of device connection 13; thence, through switch 18 and input bus 23 of input/output connections 11 to using units 10. Actuating switches 17, 18 to the alternate position connects output bus 20 to cache input bus 24, while cache output bus 25 is connected by switch 18 to using units input bus 23. Buses 24, 25 also provide for data **transfer** between cache 15 and backing store 14. In a preferred construction of the invention, backing store 14 includes a plurality of direct access storage devices (DASD), while cache 15 is an electronic random-access **memory,** preferably of the semiconductive type.

L10 ANSWER 103 OF 103 USPATFULL
AN 93:27646 USPATFULL
TI Device and method for defect handling in semi-conductor memory
IN Gross, Stephen, Mountain View, CA, United States
Norman, Robert D., San Jose, CA, United States
PA SunDisk Corporation, Santa Clara, CA, United States (U.S. corporation)
PI US 5200959 19930406
AI US 1989-422949 19891017 (7)
DT Utility
FS Granted
LN.CNT 1056
INCL INCLM: 371/021.600
INCLS: 371/010.100; 371/010.200; 371/011.100; 364/245.300; 364/285.300
NCL NCLM: **714/723.000**
NCLS: **714/008.000; 714/710.000**
IC [5]
ICM: G11C029-00
EXF 371/21.6; 371/10.1; 371/10.2; 371/11.1; 364/245.3; 364/285.3; 364/970.1
AB A solid-state memory array such as an electrically erasable programmable read only memory (EEprom) or **Flash EEprom** array is used to store sequential data in a prescribed order. The memory includes a first information list containing addresses. . . .
SUMM . . . and more specifically to a simplified scheme for accessing sequential data in a non-volatile memory such as an EEprom or **Flash EEprom** memory and handling the defects therein.
SUMM . . . (RAM), Read only Memory (ROM), Programmable read-only memory (PROM), UV Erasable PROM (UVEPROM), Electrically Erasable programmable read-only memory (EEprom) and **Flash EEprom** do not suffer from these disadvantages. However, in the case of RAM, the memory is volatile, and requires constant power. . . .
SUMM ROM, EEprom and **Flash EEprom** are all non-volatile solid state memories. They retain their memory even after power is shut down. However, ROM and PROM cannot be reprogrammed. UVPROM cannot be erased electrically. On the other hand, EEprom and **Flash EEprom** have the further advantage of being electrically writable (or programmable) and erasable. Nevertheless, conventional EEprom and **Flash EEprom** have a limited lifetime due to the endurance-related stress the device suffers each time it goes through an erase/program cycle. The endurance of a **Flash EEprom** device is its ability to withstand a given number of program/erase cycles. The physical phenomenon limiting the endurance of conventional EEprom and **Flash EEprom** devices is trapping of electrons in the active dielectric films of the device. During programming, electrons are injected from the. . . in the memory array and typically the devices are rendered unreliable after 10.sup.3 to 10.sup.4 write/erase cycles. Traditionally, EEprom and **Flash EEprom** are used in applications where semi-permanent storage of data or program is required but with a limited need for reprogramming.
SUMM . . . there is little or no provision for replacing defective cells resulting from physical defects that appear later during normal operation. **Error** corrections mainly rely on schemes using **error** correction codes (ECC) which typically correct a limited number of random errors.
SUMM Similarly for EEprom or **Flash EEprom** devices, defects initially detected after fabrication must be treated. Subsequently, ECC may be used to correct a limited number of. . .
SUMM Another way of treating defects in EEprom and **Flash EEprom** is to use schemes similar to defect remapping in disks. In the normal disk system the medium is divided into. . . defect mapping in EEprom system is disclosed in copending U.S. patent application Ser. No. 337,566, filed Apr. 13, 1989, entitled "**Flash EEprom** System." The copending application is assigned to the same assignee of the present application and the disclosure of which is. . .
SUMM It is another object of the invention to provide an EEprom or **Flash EEprom** system for storing sequential data.
SUMM . . . of the invention to provide a simplified and low cost controller only for writing sequential data in an EEprom or **Flash EEprom** system.
SUMM . . . invention to provide a simplified and low cost controller only for writing and reading sequential data in an EEprom or **Flash EEprom** system.

SUMM These and additional objects are accomplished by improvements in solid-state memory systems such as EEprom and **Flash** **EEprom** systems and techniques that allow simple and effective handling of defects, so that solid-state memory, even if having defects,. . .

SUMM One application of the present invention is in the storage of sequential data in a portable and detachable EEprom or **Flash** **EEprom** device. Examples would be in data logging, audio or image data applications. The device is in a detachable format functionally. . .

SUMM According to one aspect of the invention, a solid-state memory such as an EEprom or **Flash** **EEprom** memory array is partitioned into a user data portion and a first information list portion. The user data portion or. . .

SUMM . . . low cost controller without the need for microprocessor intelligence, and yet be able to handle defects endemic to EEprom or **Flash** **EEprom** and other solid-state memory devices.

DETD FIG. 1 illustrates a system of semiconductor memory. In the preferred embodiment, it comprises one or more non-volatile, EEprom or **Flash** **EEprom** memory devices 10, 12 managed by a controller 20 via an address/data bus 30 and a control bus 40. The. . . is only required to perform simple write operations and/or read operations on the memory devices 10, 12. The EEprom or **Flash** **EEprom** memory devices 10 or 12 may be detached from the system and be re-connected to another, full-feature system for other. . .

DETD Even after the initially detected defects are handled, the nature of the **Flash** **EEprom** device tends to have more and more cell failures with increasing write/erase cycling. ECC is used to correct a limited. . . the memory and adds the new defect to the defect list. This dynamic handling of defects, in addition to conventional **error** correction schemes, significantly increases the reliability and prolongs the life of the device.

DETD . . . is written to the next good location. Each write can be followed by a verification step. (An improved EEprom or **Flash** **EEprom** device with write-verification is also disclosed in co-pending U.S. patent application Ser. No. 337,579, and pertinent portions of which are. . .

DETD . . . at the current location of the dynamic defect list 130 as described in step (3) and operation terminates, returning an **error** status condition to the system.

DETD . . . was just written, the write operation is terminated and an Operation-Complete status is made available to the system. If an **error** condition caused the End-Of-List mark to be written prematurely, **error** status is also made available to the system.

DETD . . . or invalid entry is encountered, then the desired file is incomplete in memory. In this case, operation is terminated and **error** status is made available to the system.

CLM What is claimed is:

. . . sequential data as in claim 6, wherein said memory array is an Electrically Erasable Programmable Read Only Memory (EEprom) or **Flash** **EEprom**.

. . . sequential data as in claim 9, wherein said memory array is an Electrically Erasable Programmable Read Only Memory (EEprom) or **Flash** **EEprom**.

. . . sequential data as in claim 5, wherein said memory array is an Electrically Erasable Programmable Read Only Memory (EEprom) or **Flash** **EEprom**.

. . . sequential data as in claim 15, wherein said memory array is an Electrically Erasable Programmable Read Only Memory (EEprom) or **Flash** **EEprom**.

. . . sequential data as in claim 18, wherein said memory array is an Electrically Erasable Programmable Read Only Memory (EEprom) or **Flash** **EEprom**.

. . . sequential data as in claim 21, wherein said memory array is an Electrically Erasable Programmable Read Only Memory (EEprom) or **Flash** **EEprom**.

. . . sequential data as in claim 14, wherein said memory array is an Electrically Erasable Programmable Read Only Memory (EEprom) or **Flash** **EEprom**.

. . . sequential data as in claim 4, wherein said memory array is an Electrically Erasable Programmable Read Only Memory (EEprom) or **Flash** **EEprom**.

NCL NCLM: 714/723.0
NCLS: 714/008.0 714/710.000

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L1        1311 S MEMORY CARD/TI,AB,CLM
L2         408 S MEMORY CARD/TI
L3         408 S L1 AND L2
L4       18109 S EEPROM
L5          75 S L4 AND L3
L6        2873 S EEPROM/TI,AB,CLM
L7          21 S L3 AND L6
L8         393 S EEPROM (P) MEMORY CARD
L9        2472 S FLASH EEPROM
```

L9 ANSWER 2471 OF 2472 USPATFULL
AN 89:48205 USPATFULL
TI X-cell EEPROM array
IN Tigelaar, Howard L., Allen, TX, United States
Mitchell, Allan T., Garland, TX, United States
Riemenschneider, Bert R., Murphy, TX, United States
Paterson, James L., Richardson, TX, United States
PA Texas Instruments Incorporated, Dallas, TX, United States (U.S. corporation)
PI US 4839705 19890613
AI US 1987-133709 19871216 (7)
DT Utility
FS Granted
LN.CNT 428
INCL INCLM: 357/023.500
INCLS: 357/041.000; 357/045.000; 365/185.000
NCL NCLM: 365/185.160
NCLS: 257/320.000; 365/185.180; 365/185.260; 365/185.330
IC [4]
ICM: H01L027-04
ICS: H01L029-78; G11C011-40
EXF 357/23.5; 357/41; 357/45; 365/185
SUMM **Flash EEPROM** cells ahve recently been developed to allow the erasure of the charge on the floating gates of several EEPROM memory. . .
SUMM A principal advantage of the invention is the combination of **flash EEPROM** cell operation with X-cell technology. Each erase region is preferably coupled to four floating gate electrodes and is in turn. . .
SUMM **Flash EEPROM** cells ahve recently been developed to allow the erasure of the charge on the floating gates of several EEPROM memory cells at once. A description of such a cell may be found in F. Masuoka, et al., "A New Flash E.sup.2 PROM Cell Using Triple Polysilicon Technology," IEDM 84, page 464. Flash E.sup.2 PROM cells are advantageous over prior structures in that the time for a memory erase is considerably reduced.

SUMM A principal advantage of the invention is the combination of **flash EEPROM** cell operation with X-cell technology. Each erase region is preferably coupled to four floating gate electrodes and is in turn connected through a contact to an erase line that is further connected to other erase regions on the row. In a preferred embodiment, each common source region serves as the source for four select transistors that are disposed in spaced relationship about its perimeter. Thus, the preferred embodiment of the invention consists of a double "X"-cell topology, with one "X" compromising select transistors and another "X" compromising floating gate electrode couplings through tunnel windows to an erase region. The use of an X-cell topology in a EEPROM design may shrink the required array area by as much as 20%.

L9 ANSWER 2470 OF 2472 USPATFULL
AN 89:68137 USPATFULL
TI Nonvolatile semiconductor memory device using source of a single supply voltage
IN Terada, Yasushi, Hyogo, Japan
Nakayama, Takeshi, Hyogo, Japan
Kobayashi, Kazuo, Hyogo, Japan
PA Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan (non-U.S. corporation)
PI US 4858194 19890815
AI US 1988-154573 19880210 (7)
PRAI JP 1987-182698 19870721
DT Utility
FS Granted
LN.CNT 738
INCL INCLM: 365/203.000
INCLS: 365/189.010; 365/222.000
NCL NCLM: 365/185.250
NCLS: 365/185.230; 365/189.090; 365/222.000
IC [4]
ICM: G11C013-00
EXF 365/203; 365/189; 365/230
SUMM . . . electrode of each memory device at the time of data write cycle, which is, for example, disclosed in "A 128K **Flash EEPROM** Using Double Polysilicon Technology" by G. Samachisa, 1987 IEEE ISSS Digest of Technical Papers, pp. 76-77.
SUMM FIG. 1 is a diagram showing a schematic structure of a memory portion of a conventional nonvolatile semiconductor memory device and the relation between voltages applied to an electrode of each memory device at the time of data write cycle, which is, for example, disclosed in "A 128K **Flash EEPROM** Using Double Polysilicon Technology" by G. Samachisa, 1987 IEEE ISSS Digest of Technical Papers, pp. 76-77.

L9 ANSWER 2468 OF 2472 USPATFULL
AN 89:101007 USPATFULL
TI EPROM/**flash EEPROM** cell and array configuration
IN Lee, Wung K., San Jose, CA, United States
Chiao, Stephen S., Saratoga, CA, United States
PA Elite Semiconductor & Systems Int'l., Inc., San Jose, CA, United States (U.S. corporation)
PI US 4888734 19891219
AI US 1987-139885 19871228 (7)
DT Utility
FS Granted
LN.CNT 569
INCL INCLM: 365/185.000
INCLS: 365/104.000
NCL NCLM: 365/185.020
NCLS: 365/104.000; 365/185.160; 365/185.190; 365/185.300; 365/185.330
IC [4]
ICM: G11C011-40
EXF 365/185; 365/104; 357/23.5
TI EPROM/**flash EEPROM** cell and array configuration
AB . . . wordlines between EPROM source diffusions to achieve fuller programming isolation. This cell and array isolation configuration can be extended to **flash EEPROM** type products.
SUMM This invention relates generally to nonvolatile EPROM and **flash EEPROM** circuits, and more particularly to techniques of isolating unselected cells during programming and reading of selected cells in EPROM and **flash EEPROM** arrays.
SUMM . . . art overlapping control gate cell can be modified as described by Samachisa et al. in an article entitled "A 128K **Flash EEPROM** Using Double-Polysilicon Technology" in the IEEE Journal of Solid-State Circuits, Vol. sc-22, No. 5, Oct. 1987. The **flash EEPROM** array cells are all erased simultaneously by application of a high (19V) voltage on the drain with the source and. . . Unlike UV erasure, this usually over-erases the floating gate, leaving the floating gate with a positive charge so that the **flash EEPROM** is a (normally-on) depletion mode transistor ready to conduct leakage current when an adjacent cell is selected for programming or. . . gate 52, so neither the floating gate channel length 61 nor the control gate channel length 62 is constant. This **flash EEPROM** cell has more drawbacks than the Eitan partially self-aligned cell because the **flash EEPROM** variable floating gate channel length 61 and resulting uncontrollable MOS punch-through voltage and read current cause programming inconsistency and limit. . .
SUMM . . . efficiency and consistent programming, fast read speed, and scale-down ability without sacrificing performance for high or low density EPROM or **flash EEPROM** products.
SUMM For **flash EEPROM** (as well as EPROM) applications, to separate the commonly shared source diffusion regions of adjacent unselected cells, an extra isolation. . . adjacent cells will be blocked effectively by the extra isolation transistor in conjunction with the Vss isolation transistor. If a **flash EEPROM** cell can be designed to avoid over-erasures (to negative threshold voltages Vtl), this extra poly2 enhancement mode N-channel isolation transistor can be dispensed with, and the **flash EEPROM** array layout and read characteristics will be the same as those of the EPROM array. Thus, the invention is suitable for implementing both low or very high density and low or high speed EPROM and **flash EEPROM** products.
DRWD FIG. 5 illustrates three prior art overlapping control gate EPROM or **flash EEPROM** cells with a channel having a first portion under the floating gate and a second portion under the overlapping control. . .
DRWD FIG. 15 illustrates the invention in an alternate embodiment in high-speed PAL (R) type **Flash EEPROM** products;
DRWD FIG. 16 illustrates the invention in an embodiment as a full isolation EPROM or **flash EEPROM** array including an extra poly2 line parallel to, and in the center of, the cell's common source diffusion region; and
DRWD FIG. 17 shows the invention embodied in a **flash EEPROM** cell employing a double diffused drain junction to reduce the drain leakage current during erasure.

DETD FIGS. 15 and 16 show how this invention can be embodied in **flash EEPROM** structures 155 and 160, respectively, by adding long poly2 lines 150 parallel to the wordlines WL and in the middle . . . required high voltage on the drain during erasure can be charge-pumped from Vcc, permitting realization of a single power supply **flash EEPROM**. This new **flash EEPROM** cell can be combined with the new Vss isolation transistor to achieve very high density products. This increases **flash EEPROM** cell size by about 10% to 15%, but not to the size of the FIG. 5 prior art **flash EEPROM** cell. Field isolation by adequate spacing between source N++ diffusions can be employed instead of the extra poly2 isolation transistor,. . . this extra poly2 line can be eliminated, to yield EPROM and flash EEPROMs with essentially equivalent structures, although in practice **flash EEPROM** arrays differ slightly from EPROM arrays. The extra poly2 line 150 can be used in an EPROM array to achieve. . .

DETD FIG. 17 shows a cross-section through a **flash EEPROM** cell 170 which may be used in arrays according to this invention. This cell is similar to the FIG. 2. . .

CLM What is claimed is:
. . . adjacent rows of EEPROM cells, and are adapted to be either biased to the ground potential to better isolate unselected **flash EEPROM** transistors during selected EEPROM transistor programming, or to be biased to Vcc to reduce Vss series resistance during selected EEPROM transistor reading, or to be biased to the ground potential to block possible leakage current from un-selected over-erased **flash EEPROM** transistors during selected EEPROM transistor reading.

TI EPROM/**flash EEPROM** cell and array configuration

AB An EPROM structure incorporating Vss isolation transistors having gates on wordlines shared by respective rows of conventional self-aligned EPROM cells, and having source and drain regions connected in series between EPROM cell source regions and the ground Vss terminal. An isolation transistor becomes conductive only when an EPROM cell sharing its wordline is selected. During programming, otherwise possible leakage current through unselected cells sharing the selected bitline is blocked by the Vss isolation transistor. Only one unselected adjacent cell, which shares a common source region with the selected cell, can leak. This leakage, if properly suppressed and compensated, has no disturbance on unselected or selected cells during array programming. The EPROM cell drain punchthrough voltage and channel length can thus be reduced to obtain an EPROM cell with a low threshold voltage, low drain programming voltage, short programming time, low cell junction and bitline capacitance, and high read current. EPROM-type products can be constructed with single low power supplies, on-chip high voltage pumping and high speed read and programming. Additional rows of shared isolation transistors can be formed by adding extra poly2 lines in parallel to the wordlines between EPROM source diffusions to achieve fuller programming isolation. This cell and array isolation configuration can be extended to **flash EEPROM** type products.

SUMM This invention relates generally to nonvolatile EPROM and **flash EEPROM** circuits, and more particularly to techniques of isolating unselected cells during programming and reading of selected cells in EPROM and **flash EEPROM** arrays.

SUMM FIG. 5 further shows how a prior art overlapping control gate cell can be modified as described by Samachisa et al. in an article entitled "A 128K **Flash EEPROM** Using Double-Polysilicon Technology" in the IEEE Journal of Solid-State Circuits, Vol. sc-22, No. 5, Oct. 1987. The **flash EEPROM** array cells are all erased simultaneously by application of a high (19V) voltage on the drain with the source and gate grounded. Unlike UV erasure, this usually over-erases the floating gate, leaving the floating gate with a positive charge so that the **flash EEPROM** is a (normally-on) depletion mode transistor ready to conduct leakage current when an adjacent cell is selected for programming or reading. The cell's total channel length 60 is constantly defined by the poly2 mask (not shown) between control gate 52 left edge 51 and right edge 53. However, only the right edge 57 of poly1 floating gate 56 is self-aligned to edge 53 of poly2 control gate 52, so neither the floating gate channel length 61 nor the control gate channel length 62 is constant. This **flash EEPROM** cell has more drawbacks than the Eitan partially self-aligned cell because the **flash EEPROM** variable floating gate channel length 61 and resulting uncontrollable MOS punch-through voltage and read current cause programming inconsistency and limit scale-down of the cell.

SUMM Thus, there remains a need for shorter and more constant length channels in EPROM cells isolated from drain turn-on conditions in order to

achieve high efficiency and consistent programming, fast read speed, and scale-down ability without sacrificing performance for high or low density EPROM or **flash EEPROM** products.

SUMM For **flash EEPROM** (as well as EPROM) applications, to separate the commonly shared source diffusion regions of adjacent unselected cells, an extra isolation transistor can be employed by running an extra poly2 line in the center, and on top of, the split-common source diffusion, in parallel to the wordlines, to form an extra N-channel enhancement mode isolation transistor. In either EPROMs or flash EEPROMs with this poly2 layer tied to the ground potential during programming, and for EEPROMs during reading, any leakage current from possibly over-erased adjacent cells will be blocked effectively by the extra isolation transistor in conjunction with the Vss isolation transistor. If a **flash EEPROM** cell can be designed to avoid over-erasures (to negative threshold voltages Vtl), this extra poly2 enhancement mode N-channel isolation transistor can be dispensed with, and the **flash EEPROM** array layout and read characteristics will be the same as those of the EPROM array. Thus, the invention is suitable for implementing both low or very high density and low or high speed EPROM and **flash EEPROM** products.

DRWD FIG. 5 illustrates three prior art overlapping control gate EPROM or **flash EEPROM** cells with a channel having a first portion under the floating gate and a second portion under the overlapping control gate;

DRWD FIG. 15 illustrates the invention in an alternate embodiment in high-speed PAL (R) type **Flash EEPROM** products;

DRWD FIG. 16 illustrates the invention in an embodiment as a full isolation EPROM or **flash EEPROM** array including an extra poly2 line parallel to, and in the center of, the cell's common source diffusion region; and

DRWD FIG. 17 shows the invention embodied in a **flash EEPROM** cell employing a double diffused drain junction to reduce the drain leakage current during erasure.

DETD FIGS. 15 and 16 show how this invention can be embodied in **flash EEPROM** structures 155 and 160, respectively, by adding long poly2 lines 150 parallel to the wordlines WL and in the middle of split common source diffusions to form an additional poly2 isolation transistor with a minimum channel length, because the separation between its source and drain regions is relatively small. To achieve full isolation of adjacent cells during programming and reading, each extra poly2 line 150 is held at the ground potential, and will block leakage current from a possibly over-erased (negative Vt) cell adjacent the selected cell on the same bitline. During reading operations, the extra poly2 line 150 can be biased to Vcc to electrically remove this isolation to achieve low common source resistance for higher speed reading if the cell Vt is positive. The majority of drain current during electrical flash erasure will thus result from Fowler-Nordheim tunneling, which is very small for single cells. The required high voltage on the drain during erasure can be charge-pumped from Vcc, permitting realization of a single power supply **flash EEPROM**. This new **flash EEPROM** cell can be combined with the new Vss isolation transistor to achieve very high density products. This increases **flash EEPROM** cell size by about 10% to 15%, but not to the size of the FIG. 5 prior art **flash EEPROM** cell. Field isolation by adequate spacing between source N++ diffusions can be employed instead of the extra poly2 isolation transistor, but would increase the array size. If flash electrical erase can be controlled to avoid overerasures, this extra poly2 line can be eliminated, to yield EPROM and flash EEPROMs with essentially equivalent structures, although in practice **flash EEPROM** arrays differ slightly from EPROM arrays. The extra poly2 line 150 can be used in an EPROM array to achieve full isolation during programming. The cell programming efficiency is not degraded because a constant length short channel can be used.

DETD FIG. 17 shows a cross-section through a **flash EEPROM** cell 170 which may be used in arrays according to this invention. This cell is similar to the FIG. 2 conventional self-aligned EPROM cell except that it incorporates a double-diffused drain region to increase the drain breakdown voltage during erasure. The double diffused drain decreases leakage current at the drain junction 175 and drain surface beneath the floating gate.

3. An EPROM structure as in claim 2 wherein said EPROM transistors comprise flash EPROM transistors, additional isolation transistors are formed by an extra poly2 line formed between EEPROM transistor common source regions in the middle of said second alternate space between adjacent rows of EEPROM cells, and are adapted to be either biased to the ground potential to better isolate unselected **flash EEPROM** transistors during selected EEPROM transistor

programming, or to be biased to Vcc to reduce Vss series resistance during selected EEPROM transistor reading, or to be biased to [illegible] ground potential to block possible leakage current from un-selected over-erased **flash EEPROM** transistors during selected EEPROM transistor reading.

L9 ANSWER 2458 OF 2472 USPATFULL
AN 90:87822 USPATFULL
TI Circuit for controlling a **flash EEPROM** having three distinct modes of operation by allowing multiple functionality of a single pin
IN Ali, Syed, Cupertino, CA, United States
Cedar, Yoram, Sunnyvale, CA, United States
PA WaferScale Integration, Inc., Fremont, CA, United States (U.S. corporation)
PI US 4970692 19901113
AI US 1990-483285 19900220 (7)
RLI Continuation of Ser. No. US 1987-91917, filed on 1 Sep 1987, now abandoned
DT Utility
FS Granted
LN.CNT 535
INCL INCLM: 365/218.000
INCLS: 365/189.010; 365/189.030; 365/189.050; 365/230.020; 365/230.060
NCL NCLM: 365/230.060
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TI Circuit for controlling a **flash EEPROM** having three distinct modes of operation by allowing multiple functionality of a single pin
SUMM This invention relates to electrically erasable programmable read only memories (EEPROMs), and more specifically to flash EEPROMs. (A **flash EEPROM** is an EEPROM which has three distinct modes of operation: a read mode in which data is read from the. . . .
SUMM One type of prior art memory device is a non-**flash EEPROM**. When it is desired to program a non-**flash EEPROM**, program data is provided on the EEPROM data bus, an address is provided on the EEPROM address bus, and the. . .
SUMM Another type of memory device is the **flash EEPROM** which can enter an erase mode independently of whether the **flash EEPROM** is to be programmed, or enter the programming mode independently of whether the **flash EEPROM** is to be erased Typically, such a **flash EEPROM** includes a programming voltage pin, and when a programming voltage is asserted on the programming voltage pin, the **flash EEPROM** will go into either the erase or programming mode. It is necessary to communicate to the **flash EEPROM** whether it is desired to program or erase the **flash EEPROM**. This is typically done by the either (1) providing an extra pin on the **flash EEPROM** for providing a signal indicative or whether a programing or erase operation is desired, or (2) designing one or more of the other **flash EEPROM** pins so that if these pins receive a signal which is in excess of conventional TTL voltage levels, the **flash EEPROM** will enter the erase mode, but otherwise will enter the programming mode.
SUMM . . . . EEPROM. Accordingly, in the prior art, additional integrated circuits are required to permit a microprocessor to store data in a **flash EEPROM**.
SUMM FIG. 1 illustrates a prior art circuit 10 including a microprocessor 14 for communicating with a **flash EEPROM** 12. (Typically, other devices such as static RAMs and peripheral I/O devices are also coupled to microprocessor 14, but these. . .
SUMM It is also necessary to be able to cause **flash EEPROM** 12 to go into an erase mode to erase the data stored therein in response to signals from microprocessor 14.. . .
SUMM In accordance with one novel feature of our invention, a decoder is provided within a **flash EEPROM** for monitoring the address bus of the EEPROM. When the programming voltage VPP pin of the EEPROM is raised to. . .
DETD FIG. 2 schematically illustrates a circuit 50 including a microprocessor 52 which communicates with a **flash EEPROM** 54 in accordance with our invention. FIG. 3 illustrates the timing for the signals applied to EEPROM 54 by microprocessor. . .

TI Circuit for controlling a **flash EEPROM** having three distinct modes of operation by allowing multiple functionality [illegible] a single pin

SUMM This invention relates to electrically erasable programmable read only memories (EEPROMs), and more specifically to flash EEPROMs. (A **flash EEPROM** is an EEPROM which has three distinct modes of operation: a read mode in which data is read from the EEPROM, a programming mode in which data is stored in the EEPROM, and an erase mode in which the entire contents of the EEPROM are erased.)

SUMM One type of prior art memory device is a non-**flash EEPROM**. When it is desired to program a non-**flash EEPROM**, program data is provided on the EEPROM data bus, an address is provided on the EEPROM address bus, and the EEPROM automatically executes an erase cycle in which the selected address is erased, followed by a programming cycle, in which the selected address is loaded with the program data.

SUMM Another type of memory device is the **flash EEPROM** which can enter an erase mode independently of whether the **flash EEPROM** is to be programmed, or enter the programming mode independently of whether the **flash EEPROM** is to be erased Typically, such a **flash EEPROM** includes a programming voltage pin, and when a programming voltage is asserted on the programming voltage pin, the **flash EEPROM** will go into either the erase or programming mode. It is necessary to communicate to the **flash EEPROM** whether it is desired to program or erase the **flash EEPROM**. This is typically done by the either (1) providing an extra pin on the **flash EEPROM** for providing a signal indicative or whether a programing or erase operation is desired, or (2) designing one or more of the other **flash EEPROM** pins so that if these pins receive a signal which is in excess of conventional TTL voltage levels, the **flash EEPROM** will enter the erase mode, but otherwise will enter the programming mode.

SUMM It is known in the art to provide microprocessor systems including a microprocessor coupled to various devices such as EEPROMs, static RAMs, and peripheral I/O devices. The microprocessor provides a write control pulse to control the flow of data from the microprocessor to the devices connected thereto. Typical microprocessors are designed to communicate with devices which can store data in a very short time period. Thus, the write control pulse is generally on the order of approximately 100 nanoseconds long. However, it typically requires between several hundred microseconds and several milliseconds to store data in an EEPROM. Accordingly, in the prior art, additional integrated circuits are required to permit a microprocessor to store data in a **flash EEPROM**.

SUMM FIG. 1 illustrates a prior art circuit 10 including a microprocessor 14 for communicating with a **flash EEPROM** 12. (Typically, other devices such as static RAMs and peripheral I/O devices are also coupled to microprocessor 14, but these other devices are not shown in FIG. 1 to simplify the illustration.) The circuit of FIG. 1 is described by Samba Murthy in an article entitled "EEPROM Programs in a Flash", published in Electronic System Design Magazine in Apr. 1987, incorporated herein by reference. When it is desired to write data to EEPROM 12, microprocessor 14 provides an address on address bus 22, data on data bus 16 and a write control pulse on a write enable lead 24. Also, during write operations, the output signal on I/O output port lead 18 is active (low), and the output signal on I/O output port lead 20 is inactive (high). When the signal at lead 18 is low, a logic and switching circuit 19 raises voltage VPP from 5 to 12 volts, and the write control pulse on lead 24 is communicated to EEPROM 12 via an OR gate 13.

SUMM It is also necessary to be able to cause **flash EEPROM** 12 to go into an erase mode to erase the data stored therein in response to signals from microprocessor 14. When it is desired to erase EEPROM 12, the signal at I/O output port leads 18 and 20 go active (low), thereby causing circuit 19 to raise the voltage at VPP pin 30 and at address pins 21 of EEPROM 12 to about 12 volts. The presence of 12 volts at pins 21 is sensed by EEPROM 12, which responds by erasing the data stored therein. Unfortunately, circuit 19 represents several additional integrated circuits within circuit 10, thereby adding to the expense of circuit 10. In addition, the circuit 19 must be able to withstand high voltages, e.g. about 12 volts. Circuits of this nature tend to be slow, thereby impeding the speed of communication of addresses to EEPROM 12 and thus slowing circuit 10 during reading and writing operations.

SUMM In accordance with one novel feature of our invention, a decoder is provided within a **flash EEPROM** for monitoring the address bus of the EEPROM. When the programming voltage VPP pin of the EEPROM is raised to a high voltage, e.g. about 12 volts, the EEPROM decoder monitors the address bus for selected addresses. If, immediately after voltage VPP goes to 12 volts, the EEPROM receives a first predetermined address on the address bus (for example, address 2AAA (hexidecimal)), the decoder interprets the presence of this first predetermined address as an instruction to go into the erase mode. If, immediately after voltage VPP goes to 12 volts, the EEPROM receives a second predetermined address on the address bus (for example, address 5555 (hexidecimal)), the decoder interprets this second predetermined address as an instruction to go into the programming mode. The EEPROM then remains in either the erase mode or programming mode, as appropriate, until the voltage at the VPP pin is reduced, e.g. to 5 volts. If the EEPROM is in the programming mode, further addresses received on the address bus are interpreted as instructions to store data in the location within the EEPROM corresponding to the received address. It is noted that the above-described mechanism for controlling whether the EEPROM goes into the programming or erase modes does not require an extra pin on the EEPROM. Further, the EEPROM can be used in a circuit without requiring additional integrated circuits which drive EEPROM address lines with high voltages, and which also degrade the speed with which addresses are communicated to the EEPROM.

DETD FIG. 2 schematically illustrates a circuit 50 including a microprocessor 52 which communicates with a **flash EEPROM** 54 in accordance with our invention. FIG. 3 illustrates the timing for the signals applied to EEPROM 54 by microprocessor 52. Referring to FIGS. 2 and 3, when it is desired to program EEPROM 54 (i.e. store data in EEPROM 54), microprocessor 52 applies a control signal to a VPP voltage switch 56 via a lead 58 and a buffer 59, thereby causing switch 56 to raise the voltage at VPP pin 60 of EEPROM 54, e.g., from 5 volts to about 12 volts. Thereafter, a first address A1 (FIG. 3) is provided on the address bus 62 of EEPROM 54. Microprocessor 52 also generates a first write enable pulse 40 on a write enable lead 64. In addition, an address decoder 66 coupled to the address bus of microprocessor 52 generates a chip select signal pulse 46 on a lead 68 when microprocessor 52 accesses EEPROM 54. When the chip select and write enable pulses are present at leads 64 and 68, EEPROM 54 stores address A1 on address bus 62 in a register 100 within EEPROM 54 (FIG. 4) and presents the latched address to a decoder 102. If latched address A1 is a first predetermined address (e.g. address 2AAA (hexidecimal)), the EEPROM interprets this as an instruction to enter the programming mode. If address A1 constitutes an instruction to enter the programming mode, EEPROM 54 remains in the programming mode until voltage VPP drops back to 5 volts. If latched address A1 is a second predetermined address (e.g. address 5555 (hexidecimal)), EEPROM 54 interprets this as an instruction to enter the erase mode. If address A1 constitutes an instruction to enter the erase mode, all the data in the EEPROM is erased and the EEPROM remains in the erase mode until voltage VPP drops back to 5 volts.